

FORM PTO-1449

(REV. 7-80)

U.S. DEPARTMENT OF COMMERCE

PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO.

51889/4 US

APPLICATION NO.

10/733,612

## INFORMATION DISCLOSURE CITATION

Title: SRAM Cell



APPLICANT - Douglas R. Hackler, Sr. et al.

FILING DATE-  
December 11, 2003

Au 28 18

## OTHER DOCUMENTS (Including Author, Title, Date, Relevant Pages, Place of Publication, etc.)

TH	1	van Meer et al., "70 nm Fully-Depleted SOI CMOS Using a New Fabrication Scheme: The Spacer/Replacer Scheme," 2002 IEEE, 2002 Symposium On VLSI Technology Digest of Technical Papers, pgs. 170-171.
	2	Baze et al., "A Digital CMOS Design Technique for SEU Hardening," IEEE Transactions on Nuclear Science, Vol. 47, No. 6, December 2000, pgs. 2603-2608.
	3	Khare et al., "A High Performance 90nm SOI Technology with 0.992 $\mu\text{m}^2$ 6T-SRAM Cell," 2002 IEEE, pgs. 16.1.1-16.1.4.
	4	Ootsuka et al., "A Novel 0.20 $\mu\text{m}$ Full CMOS SRAM Cell Using Stacked Cross Couple with Enhanced Soft Error Immunity," 1998 IEEE, pgs. 8.3.1-8.3.4.
	5	Cox et al., "A Partially Depleted 1.8V SOI CMOS SRAM Technology Featuring a 3.77 $\mu\text{m}^2$ Cell," 2000 IEEE, 2000 Symposium on VLSI Technology Digest of Technical Papers, pgs. 170-171.
	6	Ikeda et al., "A Soft Error Immune 0.35 $\mu\text{m}$ PD-SOI SRAM Technology Compatible with Bulk CMOS," Proceedings 1998 IEEE International SOI Conference, October 1998, pgs. 159-160.
	7	Warren et al., "Analysis of the Influence of MOS Device Geometry on Predicted SEU Cross Sections," IEEE Transactions on Nuclear Science, Vol. 46, No. 6, December 1999, pgs. 1363-1369.
	8	Dodd et al., "Basic Mechanisms and Modeling of Single-Event Upset in Digital Microelectronics," IEEE Transactions on Nuclear Science, Vol. 50, No. 3, June 2003, pgs. 583-602.
	9	Schwank et al., "BUSFET - A Radiation-Hardened SOI Transistor," IEEE Transactions on Nuclear Science, Vol. 46, No. 6, December 1999, pgs. 1809-1816.
	10	Shaneyfelt et al., "Challenges in Hardening Technologies Using Shallow-Trench Isolation," IEEE Transactions on Nuclear Science, Vol. 45, No. 6, December 1998, pgs. 2584-2592.
	11	Gasiot et al., "Comparison of the Sensitivity to Heavy Ions of 0.25- $\mu\text{m}$ Bulk and SOI Technologies," IEEE Transactions on Nuclear Science, Vol. 49, No. 3, June 2002, pgs. 1450-1455.
	12	Sung et al., "Design of an Embedded Fully-Depleted SOI SRAM," 2001 IEEE, pgs. 13-18.
	13	Zhang et al., "Double-Gate Fully-Depleted SOI Transistors for Low-Power High-Performance Nano-Scale Circuit Design," pgs. 213-218.
	14	Brady et al., "Evaluation of the Performance and Reliability of a 1M SRAM on Fully-Depleted SOI," Proceedings 1998 IEEE International SOI Conference, October 1998, pgs. 129-130.
	15	Hirano et al., "High Soft-Error Tolerance Body-Tied SOI Technology with Partial Trench Isolation (PTI) for Next Generation Devices," 2002 IEEE, 2002 Symposium On VLSI Technology Digest of Technical Papers, pgs. 48-49.
	16	Hirano et al., "Impact of Actively Body-bias Controlled (ABC) SOI SRAM by using Direct Body Contact Technology for Low-Voltage Application," 2003 IEEE, pgs. 2.4.1-2.4.4.
TH	17	Hazucha et al., "Impact of CMOS Technology Scaling on the Atmospheric Neutron Soft Error Rate," IEEE Transactions on Nuclear Science, Vol. 47, No. 6, December 2000, pgs. 2586-2594.

EXAMINER

TH-TH-HO

DATE CONSIDERED

Feb. 2005

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449  
(REV. 7-80)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
51889/4 USAPPLICATION NO.  
10/733,612

## INFORMATION DISCLOSURE CITATION

Title: SRAM Cell



APPLICANT - Douglas R. Hackler, Sr. et al.

FILING DATE-  
December 11, 2003

EXAMINER

DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

TH	18	Leray et al., "Impact of Technology Scaling in SOI Back-Channel Total Dose Tolerance, a 2-D Numerical Study Using Self-Consistent Oxide Code," IEEE Transactions on Nuclear Science, Vol. 47, No. 3, June 2000, pgs. 620-626.
	19	Tosaka et al., "Measurement and Analysis of Neutron-Induced Soft Errors in Sub-Half-Micron CMOS Circuits," IEEE Transactions on Electron Devices, Vol. 45, No. 7, July 1998, pgs. 1453-1458.
	20	Sexton et al., "Precursor Ion Damage and Angular Dependence of Single Event Gate Rupture in Thin Oxides," IEEE Transactions on Nuclear Science, Vol. 45, No. 6, December 1998, pgs. 2509-2518.
	21	Liu et al., "Proton Induced Single Event Upset In A 4M SOI SRAM," 2003 IEEE, pgs. 26-27.
	22	Schwank et al., "Radiation Effects in SOI Technologies," IEEE Transactions on Nuclear Science, Vol. 50, No. 3, June 2003, pgs. 522-538.
	23	Hirose et al., "SEU Resistance in Advanced SOI-SRAMs Fabricated by Commercial Technology Using a Rad-Hard Circuit Design," IEEE Transactions on Nuclear Science, Vol. 49, No. 6, December 2002, pgs. 2965-2968.
	24	Dodd et al., "SEU-Sensitive Volumes in Bulk and SOI SRAMs From First-Principles Calculations and Experiments," IEEE Transactions on Nuclear Science, Vol. 48, No. 6, December 2001, pgs. 1893-1903.
	25	Gasiot et al., "SEU Sensitivity of Bulk and SOI Technologies to 14-MeV Neutrons," IEEE Transactions on Nuclear Science, Vol. 49, No. 6, December 2002, pgs. 3032-3037.
	26	Dodd et al., "Single-Event Upset and Snapback in Silicon-on-Insulator Devices and Integrated Circuits," IEEE Transactions on Nuclear Science, Vol. 47, No. 6, December 2000, pgs. 2165-2174.
	27	Cohen et al., "Soft Error Considerations for Deep-Submicron CMOS Circuit Applications," 1999 IEEE, pgs. 13.1.1-13.1.4.
	28	Milanowski et al., "TCAD-Assisted Analysis of Back-Channel Leakage in Irradiated Mesa SOI nMOSFETs," IEEE Transactions on Nuclear Science, Vol. 45, No. 6, December 1998, pgs. 2593-2599.
	29	Ferlet-Cavrois et al., "Total Dose Induced Latch in Short Channel NMOS/SOI Transistors," IEEE Transactions on Nuclear Science, Vol. 45, No. 6, December 1998, pgs. 2458-2466.
TH	30	Ferlet-Cavrois et al., "Worst-Case Bias During Total Dose Irradiation of SOI Transistors," IEEE Transactions on Nuclear Science, Vol. 47, No. 6, December 2000, pgs. 2183-2188.
	31	
	32	

EXAMINER

TV - Re Ho

DATE CONSIDERED

Feb, 2005

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<b>INFORMATION DISCLOSURE CITATION</b> (Use several sheets if necessary)				Docket Number (Optional)		Application Number		
				51889/4		10/733,612		
				Applicant(s)				
				Douglas R. Hackler, Sr. et al.				
Filing Date		Group Art Unit						
December 11, 2003		2818						
<b>U.S. PATENT DOCUMENTS</b>								
EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE	
TH	A1	2003/0058001	03/27/03	Boerstler et al.	326	113	09/27/01	
	A2	2002/0180486	12/05/02	Yamashita et al.	326	113	06/25/02	
	A3	2002/0084803	07/04/02	Mathew et al.	326	113	12/29/00	
	A4	2002/0081808	06/27/02	Forbes	438	283	01/25/02	
	A5	2002/0047727	04/25/02	Mizuno	326	113	10/18/01	
	A6	2001/0022521	09/20/01	Sasaki et al.	326	113	05/21/01	
	A7	6,433,609	08/13/02	Voldman	327	313	11/19/01	
	A8	6,420,905	07/16/02	Davis et al.	326	113	09/07/00	
	A9	6,404,237	06/11/02	Mathew et al.	326	113	12/29/00	
	A10	6,376,317	04/23/02	Forbes et al.	438	283	06/28/00	
TH	A11	6,188,243	02/13/01	Liu et al.	326	81	06/09/99	
<b>FOREIGN PATENT DOCUMENTS</b>								
	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO
<b>OTHER DOCUMENTS</b> (Including Author, Title, Date, Pertinent Pages, Etc.)								
EXAMINER				DATE CONSIDERED				
TH TH HO				Feb, 2005				

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

**INFORMATION DISCLOSURE CITATION**  
(Use several sheets if necessary)

ATTY DOCKET NO.  
51889/4

SERIAL NO.  
10/733,612

Douglas R. Hackler, Sr. et al.

FILING  
December 11, 2003

GROUP

**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
TH	A12	6,104,068	08/15/00	Forbes	257	365	09/01/98
	A13	6,097,221	08/01/00	Sako	326	113	12/10/96
	A14	6072,354	06/06/00	Tachibana et al.	327	390	09/29/97
	A15	4,468,574	08/28/84	Engeler et al.	307	451	05/03/82
TH	A16	4,300,064	11/10/81	Eden	307	446	02/12/79

**FOREIGN PATENT DOCUMENTS**

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

**OTHER DOCUMENTS** (Including Author, Title, Date, Pertinent Pages, Etc.)


EXAMINER *TR-TR HCO*

DATE CONSIDERED *Feb. 2005*

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449

(REV. 7-80)

U.S. DEPARTMENT OF COMMERCE

PATENT AND TRADEMARK OFFICE

ATTY. DOCKET NO.

51889/4 US

APPLICATION NO.

10/733,612

## INFORMATION DISCLOSURE CITATION

Title: SRAM Cell



APPLICANT - Douglas R. Hackler, Sr. et al.

FILING DATE-  
December 11, 2003

Au 2818

## U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
TH	1	2002/0187610 A1	12/12/02	Furukawa et al.	438	283	06/12/01
	2	2002/0153587 A1	10/24/02	Adkisson et al.	257	510	07/02/02
	3	2002/0140039 A1	10/03/02	Adkisson et al.	257	377	06/18/02
	4	2002/0105039 A1	08/08/02	Hanafi et al.	257	401	02/07/01
	5	2002/0093053 A1	07/18/02	Chan et al.	257	347	01/18/02
	6	2003/0089930 A1	05/15/03	Zhao	257	256	11/07/02
	7	6,580,137 B2	06/17/03	Parke	257	401	08/29/01
	8	6,518,127 B2	02/11/03	Hshieh et al.	438	270	06/01/01
	9	6,506,638 B1	01/14/03	Yu	438	156	10/12/00
	10	6,483,156 B1	11/19/02	Adkisson et al.	257	401	03/16/00
	11	6,472,258 B1	10/29/02	Adkisson et al.	438	192	11/13/00
	12	6,365,465 B1	04/02/02	Chan et al.	438	283	03/19/99
	13	6,064,589	05/16/00	Walker	365	149	05/05/98
	14	5,773,331	06/30/98	Solomon et al.	438	164	12/17/96
	15	5,677,550	10/14/97	Lee	257	69	04/15/93
TH	16	5,436,506	07/25/95	Kim et al.	257	347	10/12/93

EXAMINER

TU-TU HO

DATE CONSIDERED

Feb. 2005

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449  
(REV. 7-80)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
51889/4 US.APPLICATION NO.  
10/733,612

## INFORMATION DISCLOSURE CITATION

Title: SRAM Cell

APPLICANT - Douglas R. Hackler, Sr. et al.

FILING DATE-  
December 11, 2003

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
TH	17	5,349,228	09/20/94	Neudeck et al.	257	365	12/07/93
TH	18	5,273,921	12/28/93	Neudeck et al.	437	41	12/27/91
TH	19	3,755,012	08/28/73	George et al.	148	175	03/19/71

## FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICA- TION DATE	COUNTRY / PATENT OFFICE	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
	20							
	21							
	22							
	23							
	24							
	25							
	26							
	27							

## OTHER DOCUMENTS (Including Author, Title, Date, Relevant Pages, Place of Publication, etc.)

TH	28	Harada et al., "2-GHz RF Front-End Circuits in CMOS/SIMOX Operating at an Extremely Low Voltage of 0.5 V," IEEE Journal of Solid-State Circuits, Vol. 35, No. 12, December 2000, pgs. 2000-2004.
TH	29	Wann et al., "CMOS with Active Well Bias for Low-Power and RF/Analog Applications," 2000 Symposium on VLSI Technology Digest of Technical Papers, 2 pgs.
TH	30	Yang et al., "Back-Gated CMOS on SOI for Dynamic Threshold Voltage Control," IEEE Transactions on Electron Devices, Vol. 44, No. 5, May 1997, pgs. 822-831.
TH	31	Assaderaghi et al., "Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI," IEEE Transactions on Electron Devices, Vol. 44, No. 3, March 1997, pgs. 414-422.

EXAMINER

TH - TH - TH

DATE CONSIDERED

Feb, 2005

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449  
(REV. 7-80)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
51889/4 USAPPLICATION NO.  
10/733,612

## INFORMATION DISCLOSURE CITATION

Title: SRAM Cell

APPLICANT – Douglas R. Hackler, Sr. et al.

FILING DATE-  
December 11, 2003

TH	32	Assaderaghi et al., "A Dynamic Threshold Voltage MOSFET (DTMOS) for Very Low Voltage Operation," IEEE Electron Device Letters, Vol. 15, No. 12, December 1994, pgs. 510-512.
	33	Assaderaghi et al., "A Dynamic Threshold Voltage MOSFET (DTMOS) for Ultra-Low Voltage Operation," Department of Electrical Engineering and Computer Science, University of California at Berkeley, Berkeley, CA, pgs. 33.1.1-33.1.4.
	34	Hsu et al., "Low-Frequency Noise Properties of Dynamic-Threshold (DT) MOSFET's," IEEE Electron Device Letters, Vol. 20, No. 10, October 1999, pgs. 532-534.
	35	Wong, H.-S. Philip, "Field Effect Transistors – From Silicon MOSFETs to Carbon Nanotube FETs," Proc. 23 <sup>rd</sup> International Conference on Microelectronics (Miel 2002), Vol. 1, NIS, Yugoslavia, 12-15 May, 2002, pgs. 103-107.
	36	Brown et al., "Intrinsic Fluctuations in Sub 10-nm Double-Gate MOSFETs Introduced by Discreteness of Charge and Matter," IEEE Transactions on Nanotechnology, Vol. 1, No. 4, December 2002, pgs. 195-200.
	37	Denton et al., "Fully Depleted Dual-Gated Thin-Film SOI P-MOSFET's Fabricated in SOI Islands with an Isolated Buried Polysilicon Backgate," IEEE Electron Device Letters, Vol. 17, No. 11, November 1996, pgs. 509-511.
	38	Doris et al., "Extreme Scaling with Ultra-Thin Si Channel MOSFETs," IBM Semiconductor Research and Development Center (SRDC), Microelectronics Division, Hopewell Junction, NY 12533, pgs. 10.6.1-10.6.4.
	39	Choi et al., "Nanoscale Ultrathin Body PMOSFETs With Raised Selective Germanium Source/Drain," IEEE Electron Device Letters, Vol. 22, No. 9, September 2001, pgs. 447-448.
	40	Uchida et al., "Experimental Evidences of Quantum-Mechanical Effects on Low-field Mobility, Gate-channel Capacitance, and Threshold Voltage of Ultrathin Body SOI MOSFETs," Advanced LSI Technology Laboratory, Toshiba Corp., 8 Shinsugita-cho, Isogo-ku Yokohama 235-8522, Japan, pgs. 29.4.1-29.4.4.
	41	Ren et al., "An Experimental Study on Transport Issues and Electrostatics of Ultrathin Body SOI pMOSFETs," IEEE Electron Device Letters, Vol. 23, No. 10, October 2002, pgs. 609-611.
	42	Colinge et al., "Silicon-On-Insulator 'Gate-All-Around Device'," IMEC, Kapeldreef 75, 3030 Leuven, Belgium, pgs. 25.4.1-25.4.4.
	43	Hergenrother et al., "50 nm Vertical Replacement-Gate (VRG) nMOSFETs with ALD HfO <sub>2</sub> and Al <sub>2</sub> O <sub>3</sub> Gate Dielectrics," Agere Systems, Murray Hill, NJ 07974, USA, pgs. 3.1.1-3.1.4.
	44	Hokazono et al., "14 nm Gate Length CMOSFETs Utilizing Low Thermal Budget Process with Poly-SiGe and Ni Salicide," SoC Research & Development Center, Process & Manufacturing Engineering Center, <sup>2</sup> System LSI Division, Toshiba Corporation Semiconductor Company, 8 Shinsugita-cho, Isogo-ku, Yokohama, Kanagawa 235-8522, Japan, pgs. 27.1.1-27.1.4.
	45	Schulz et al., "50-nm Vertical Sidewall Transistors With High Channel Doping Concentrations," Infineon Technologies AG, Corporate Research, D-81730 Munich, Germany, pgs. 3.5.1-3.5.4.
TH	46	Fung et al., "Gate length scaling accelerated to 30nm regime using ultra-thin film PD-SOI Technology," IBM Microelectronics Semiconductor Research and Development Center (SRDC), pgs. 29.3.1-29.3.4.

EXAMINER

TU STE HO

DATE CONSIDERED

Feb 2005

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449  
(REV. 7-80)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
51889/4 US.APPLICATION NO.  
10/733,612

## INFORMATION DISCLOSURE CITATION

Title: **SRAM Cell**

APPLICANT – Douglas R. Hackler, Sr. et al.

FILING DATE-  
December 11, 2003

TH	47	Narasimha et al., "High Performance Sub-40nm CMOS Devices on SOI for the 70nm Technology Node," IBM Microelectronics Semiconductor Research and Development Center (SRDC), Hopewell Junction, NY 12533, USA, pgs. 29.2.1-29.2.4.
	48	Hisamoto, Digh, "FD/DG-SOI MOSFET – a viable approach to overcoming the device scaling limit," Central Research Laboratory, Hitachi Ltd., Kokubunji, Tokyo 185-8601, Japan, pgs. 19.3.1-19.3.4.
	49	Kedzierski et al., "Complementary silicide source/drain thin-body MOSFETs for the 20nm gate length regime," Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA, 94720, USA, pgs. 3.4.1-3.4.4.
	50	Oh et al., "50 nm Vertical Replacement-Gate (VRG) pMOSFETs," Bell Laboratories, Lucent Technologies, Murray Hill, NJ 07974, USA, pgs. 3.6.1-3.6.4.
	51	Pidin et al., "A Notched Metal Gate MOSFET for sub-0.1 $\mu$ m Operation," Fujitsu Laboratories Ltd., 10-1 Morinosato-Wakamiya, Atsugi 243-0197, Japan, pgs. 29.1.1-29.1.4.
	52	Tavel et al., "High Performance 40nm nMOSFETs With HfO <sub>2</sub> Gate Dielectric and Polysilicon Damascene Gate," France Telecom R&D, B.P. 98, 38243 Meylan, France, pgs. 17.1.1-17.1.4.
	53	Krivokapic et al., "Nickel Silicide Metal Gate FDSOI Devices with Improved Gate Oxide Leakage," AMD, Technology Research Group, M/S 143, One AMD Place, Sunnyvale, CA 94088-3453, USA, pgs. 10.7.1-10.7.4.
	54	Monfray et al., "SON (Silicon-On-Nothing) P-MOSFETs with totally silicided (CoSi <sub>2</sub> ) Polysilicon on 5nm-thick Si-films: The simplest way to integration of Metal Gates on thin FD channels," ST Microelectronics, 850, rue J.Monnet, 38921 Crolles, France, pgs. 10.5.1-10.5.4.
	55	Yang et al., "25 nm CMOS Omega FETs," Taiwan Semiconductor Manufacturing Company, No. 6, Li-Hsin Rd. 6, Science-Based Industrial Park, Hsin-Chu, Taiwan, ROC, pgs. 10.3.1-10.3.4.
	56	Wong et al., "Design and Performance Considerations for Sub-0.1 $\mu$ m Double-Gate SOI MOSFET's," I.B.M. Thomas J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598, U.S.A., pgs. 30.6.1-30.6.4.
	57	Wong et al., "Device Design Considerations for Double-Gate, Ground-Plane, and Single-Gated Ultra-Thin SOI MOSFET's at the 25 nm Channel Length Generation," IBM T.J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598, U.S.A., pgs. 15.2.1-15.2.4.
	58	Guarini et al., "Triple-Self-Aligned, Planar Double-Gate MOSFETs: Devices and Circuits," IBM T.J. Watson Research Center, Yorktown Heights, New York 10598, U.S.A., pgs. 19.2.1-19.2.4.
	59	Solomon et al., "Two Gates Are Better Than One," IEEE Circuits & Devices Magazine, January 2003, pgs. 48-63.
	60	Cheng et al., "The Impact of High- $\kappa$ Gate Dielectrics and Metal Gate Electrodes on Sub-100 nm MOSFET's," IEEE Transactions on Electron Devices, Vol. 46, No. 7, July 1999, pgs. 1537-1544.
TH	61	Oh et al., "Analytic Description of Short-Channel Effects in Fully-Depleted Double-Gate and Cylindrical, Surrounding-Gate MOSFETs," IEEE Electron Device Letters, Vol. 21, No. 9, September 2000, pgs. 445-447.

EXAMINER

TH-TH-110

DATE CONSIDERED

Feb. 2005

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.



FORM PTO-1449  
(REV. 7-80)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
51889/4 USAPPLICATION NO.  
10/733,612

## INFORMATION DISCLOSURE CITATION

Title: **SRAM Cell**

APPLICANT – Douglas R. Hackler, Sr. et al.

FILING DATE-  
December 11, 2003

76	62	Jeong et al., "High Performance Double-Gate Device Technology Challenges and Opportunities," IBM Microelectronics Semiconductor Research and Development Center (SRDC), Hopewell Junction, NY, USA, pgs. 492-495.
	63	Chang et al., "Gate Length Scaling and Threshold Voltage Control of Double-Gate MOSFETs," Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720, USA, pgs. 31.2.1-31.2.4.
	64	Wong et al., "Self-Aligned (Top and Bottom) Double-Gate MOSFET with a 25 nm Thick Silicon Channel," IBM T. J. Watson Research Center, P.O. Box 218, Yorktown Heights, New York 10598, U.S.A., pgs. 16.6.1-16.6.4.
	65	Yagishita et al., "Dynamic Threshold Voltage Damascene Metal Gate MOSFET (DT-DMG-MOS) with Low Threshold Voltage, High Drive Current, and Uniform Electrical Characteristics," Process & Manufacturing Engineering Center, Semiconductor Company, Toshiba Corporation, 8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan, pgs. 29.2.1-29.2.4.
	66	Samavedam et al., "Dual-Metal Gate CMOS with HfO <sub>2</sub> Gate Dielectric," Motorola Digital DNA™ Laboratories, 3501 Ed Bluestein Blvd., MD-K10, (*AMD), Austin, TX 78721, USA, pgs. 17.2.1-17.2.4.
	67	Fossum et al., "Speed Superiority of Scaled Double-Gate CMOS," IEEE Transactions on Electron Devices, Vol. 49, No. 5, May 2002, pgs. 808, 809, 811.
	68	Lee et al., "Super Self-Aligned Double-Gate (SSDG) MOSFETs Utilizing Oxidation Rate Difference and Selective Epitaxy," Microsystems Technology Laboratories, Massachusetts Institute of Technology, Cambridge, MA, USA, pgs. 3.5.1-3.5.4.
	69	Polishchuk et al., "Dual Work Function Metal Gate CMOS Technology Using Metal Interdiffusion," IEEE Electron Device Letters, Vol. 22, No. 9, September 2001, pgs. 444-446.
	70	Yeo et al., "Dual-Metal Gate CMOS Technology with Ultrathin Silicon Nitride Gate Dielectric," IEEE Electron Device Letters, Vol. 22, No. 5, May 2001, pgs. 227-229.
	71	Wakabayashi et al., "A Dual-Metal Gate CMOS Technology Using Nitrogen-Concentration-Controlled TiNx Film," IEEE Transactions on Electron Devices, Vol. 48, No. 10, October 2001, pgs. 2363-2369.
	72	Yagishita et al., "Dynamic Threshold Voltage Damascene Metal Gate MOSFET (DT-DMG-MOS) Technology for Very Low Voltage Operation of Under 0.7 V," IEEE Transactions on Electron Devices, Vol. 49, No. 3, March 2002, pgs. 422-428.
	73	Matsuo et al., "High Performance Damascene Gate CMOSFETs with Recessed Channel Formed by Plasma Oxidation and Etching Method (RC-POEM)," Process & Manufacturing Engineering Center, Semiconductor Company, Toshiba Corporation, 8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan, pgs. 17.5.1-17.5.4.
77	74	Ducroquet et al., "Full CMP Integration of CVD TiN Damascene Sub-0.1-μm Metal Gate Devices For ULSI Applications," IEEE Transactions on Electron Devices, Vol. 48, No. 8, August 2001, pgs. 1816-1821.

EXAMINER

DATE CONSIDERED

Feb. 2005

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449  
(REV. 7-80)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
51889/4 USAPPLICATION NO.  
10/733,612

## INFORMATION DISCLOSURE CITATION

Title: **SRAM Cell**

APPLICANT – Douglas R. Hackler, Sr. et al.

FILING DATE-  
December 11, 2003

TH	75	Choi et al., "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pgs. 25-27.
	76	Lindert et al., "Sub-60-nm Quasi-Planar FinFETs Fabricated Using a Simplified Process," IEEE Electron Device Letters, Vol. 22, No. 10, October 2001, pgs. 487-489.
	77	Choi et al., "A Spacer Patterning Technology for Nanoscale CMOS," IEEE Transactions on Electron Devices, Vol. 49, No. 3, March 2002, pgs. 436-441.
	78	Li et al., "Damascene W/TiN Gate MOSFETs With Improved Performance for 0.1- $\mu$ m Regime," IEEE Transactions on Electron Devices, Vol. 49, No. 11, November 2002, pgs. 1891-1896.
	79	Huang et al., "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pgs. 880-886.
	80	Pei et al., "FinFET Design Considerations Based on 3-D Simulation and Analytical Modeling," IEEE Transactions on Electron Devices, Vol. 49, No. 8, August 2002, pgs. 1411-1419.
	81	Hisamoto et al., "FinFET—A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pgs. 2320-2325.
	82	Chang et al., "FinFET Scaling to 10nm Gate Length," Strategic Technology, Advanced Micro Devices, Inc., Sunnyvale, CA 94088, USA, pgs. 10.2.1-10.2.4
	83	Choi et al., "FinFET Process Refinements for Improved Mobility and Gate Work Function Engineering," Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720, USA, pgs. 10.4.1-10.4.4.
	84	Lindert et al., "Sub-60-nm Quasi-Planar FinFETs Fabricated Using a Simplified Process," IEEE Electron Device Letters, Vol. 22, No. 10, October 2001, pgs. 487-489.
	85	Huang et al., "Sub 50-nm FinFET: PMOS," Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, CA 94720, USA, pgs. 3.4.1-3.4.4.
	86	Choi et al., "Sub-20nm CMOS FinFET Technologies," Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720, USA, pgs. 19.1.1-19.1.4.
	87	Kedzierski et al., "Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation," IBM Semiconductor Research and Development Center (SRDC), Research Division, T J Watson Research Center, Yorktown Heights, NY 10598, pgs. 10.1.1-10.1.4.
	88	Lin et al., "High-Performance P-Channel Schottky-Barrier SOI FinFET Featuring Self-Aligned PtSi Source/Drain and Electrical Junctions," IEEE Electron Device Letters, Vol. 24, No. 2, February 2003, pgs. 102-104.
	89	Lee et al., "Hydrogen Annealing Effect on DC and Low-Frequency Noise Characteristics in CMOS FinFETs," IEEE Electron Device Letters, Vol. 24, No. 3, March 2003, pgs. 186-188.
	90	Yagishita et al., "High Performance Metal Gate MOSFETs Fabricated by CMP for 0.1 $\mu$ m Regime," Microelectronics Engineering Laboratory, Toshiba Corporation, 8, Shinsugita-cho, Isogo-ku, Yokohama 235-8522, Japan, pgs. 29.3.1-29.3.4.
TH	91	Yagishita et al., "Improvement of Threshold Voltage Deviation in Damascene Metal Gate Transistors," IEEE Transactions on Electron Devices, Vol. 48, No. 8, August 2001, pgs. 1604-1611.

EXAMINER

TU-TU HO

DATE CONSIDERED

Feb, 2005

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449  
(REV. 7-80)U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. DOCKET NO.  
51889/4 USAPPLICATION NO.  
10/733,612

## INFORMATION DISCLOSURE CITATION

Title: SRAM Cell

APPLICANT - Douglas R. Hackler, Sr. et al.

FILING DATE-  
December 11, 2003

TH	92	Yahishita et al., "High Performance Damascene Metal Gate MOSFET's for 0.1 $\mu$ m Regime," IEEE Transactions on Electron Devices, Vol. 47, No. 5, May 2000, pgs. 1028-1034.
	93	Kimura et al., "Short-Channel-Effect-Suppressed Sub-0.1- $\mu$ m Grooved-Gate MOSFET's with W Gate," IEEE Transactions on Electron Devices, Vol. 42, No. 1, January 1995, pgs. 94-100.
	94	Tanaka et al., "Simulation of Sub-0.1- $\mu$ m MOSFET's with Completely Suppressed Short-Channel Effect," IEEE Electron Device Letters, Vol. 14, No. 8, August 1993, pgs. 396-399.
	95	Tanaka et al., "A Sub-0.1- $\mu$ m Grooved Gate MOSFET with High Immunity to Short-Channel Effects," Central Research Laboratory, Hitachi, Ltd., 1-280 Higashi-koigakubo, Kokubunji, Tokyo 185, Japan, pgs. 21.1.1-21.1.4.
	96	Sunouchi et al., "Double LDD Concave (DLC) Structure for Sub-Half Micron MOSFET," ULSI Research Center, Toshiba Corporation, 1, Komukai, Saiwai-ku, Kawasaki 210, Japan, pgs. 226-228.
TH	97	Hackler, Sr., Douglas R., "TMOS: A Novel Design for MOSFET Technology," A Thesis Presented in Partial Fulfillment of the Requirements for the Degree of Master of Science with a Major in Electrical Engineering in the College of Graduate Studies, University of Idaho, October 1999, 126 pgs.
	98	
	99	
	100	
	101	
	102	
	103	
	104	
	105	
	106	
	107	
	108	
	109	
	110	
	111	
	112	
	113	

EXAMINER

TL-TL HO

DATE CONSIDERED

Feb. 2005

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.